



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,766	04/02/2004	Byung Chul Ahn	8733.1048.00-US	9943
30827	7590	09/12/2006	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			CHOWDHURY, TARIFUR RASHID	
			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/815,766

Applicant(s)

AHN, BYUNG CHUL

Examiner

Tarifur R. Chowdhury

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8-20, 23, 25 and 26 is/are rejected.
- 7) ☒ Claim(s) 6, 7, 21, 22, 24 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1-5, 8-14-20, 23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Muramatsu, USPAT 6,151,091.**

3. The AAPA described in the instant application discloses (page 3, paragraph 0009 – page 12, paragraph 0036) and shows in Figs. 1-3, a liquid crystal display of horizontal electric field applying type comprising:

- a thin film transistor array substrate (45) (Fig. 2), wherein the thin film transistor array substrate includes an effective display area having a gate line (2), a common line (16) parallel to the gate line, a data line (4) crossing and isolated from the gate line and the common line with a gate insulating film (46) therebetween to define a pixel area, a thin film transistor (6) formed on each intersection of the gate line and the data line, a passivation film (52) for protecting the thin film transistor, a common electrode (18) formed in the pixel area and connected to the common line and a pixel electrode (14) connected to the thin film transistor and formed to produce horizontal electric field along with the common electrode in the pixel area, and a pad area having a gate

Art Unit: 2871

pad (24) formed to have at least one conductive layer included in the gate line, a data pad (30) formed with at least one conductive layer included in the data line, and a common pad (36) to have at least one conductive layer included in the common line;

- a color filter array substrate facing the thin film transistor array substrate as facing each other (not shown);
- a driving integrated circuit mounted on the thin film transistor array substrate in order to directly connect to any one of the gate pad and the data pad (not shown);

The AAPA described in the instant application differs from the claimed invention because it does not explicitly disclose the claimed package mold material for capsulating the pads and the driving integrated circuit.

Muramatsu discloses a liquid crystal display panel wherein a driving integrated circuit (15) and the pads are capsulated by a package mold material (21) (Fig. 2).

Lee is evidence that ordinary workers in the art would find a reason, suggestion or motivation to form a package mold material for capsulating the pads and the driving integrated circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the liquid crystal display of the AAPA by forming a package mold material for capsulating the pads and the driving integrated circuit so that the LCD driver integrated circuit package is prevented from any

Art Unit: 2871

undesirable deteriorations and thus display quality is improved and a liquid crystal display device permitting a simplified production process is obtained.

Accordingly, claim 1 would have been obvious.

As to claim 2, even though the AAPA does not explicitly disclose or show that the passivation film is removed from the pad region, it is common and known in the art to etch the passivation film from the pad region in order to connect the pads to the driving circuit and thus would have been obvious.

As to claims 3 and 4, a driver integrated circuit including a gate driving integrated circuit connected to the gate pad and a data driving integrated circuit connected to the data pad is common and known in the art and thus would have at least been obvious to supply signal to gate and data lines.

As to claims 5 and 20, a display device including a plurality of signal supplying lines is common and known in the art and thus would have been obvious to supply a driving signal to the driving integrated circuit.

As to claims 8 and 11, the AAPA described in the instant application also shows in Figs. 1-3 that the each of the gate line, common line and the data line includes a main conductive layer and a subsidiary conductive layer for providing against an opening of the main conductive layer.

As to claims 9, 10, 12 and 13, the AAPA described in the instant application also shows in Figs. 1-3 that each of the gate pad, data pad and the common pad includes a main conductive layer and a subsidiary conductive layer and wherein the subsidiary conductive layer has an exposed structure.

As to claim 15, even though the AAPA does not explicitly disclose that the drain electrode and the pixel electrode are made of an identical conductive layer, it is the most desired practice in the art is to reduce costs and one way of reducing cost is to reduce manufacturing steps and forming the pixel electrode and the drain electrode of identical material would reduce manufacturing steps and thus costs and thus would have been obvious.

As to claims 17-19, the method of fabricating the liquid crystal display merely discloses the step of forming each element and since each element must be formed to make the device, the method would have at least been obvious in view of the device.

As to claims 14, 16 and 23, it is also shown in Fig. 3A of the AAPA that the thin film transistor comprises:

- a gate electrode (8) connected to the gate line;
- a source electrode (10) connected to the data line;
- a drain electrode (12) facing the source electrode; and
- a semiconductor layer (48) overlapped with the gate electrode with the gate insulating film (46) therebetween to form a channel portion between the source electrode and the drain electrode and that the semiconductor layer is formed along the data line, the source electrode, the drain electrode and the pixel electrode.

As to claims 25 and 26, the AAPA described in the instant application also discloses that at least one of the first and the second conductive pattern group is formed to have a double-layer structure having a main conductive layer and a subsidiary

Art Unit: 2871

conductive layer for providing against the opening of the main conductive layer and that the step of exposing the gate pad and the data pad includes exposing the subsidiary conductive layers of the gate pad and the common pad and the subsidiary conductive layer of the data pad.

Allowable Subject Matter

4. Claims 6, 7, 21, 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed on June 06, 2006 have been fully considered but they are not persuasive.

In response to applicant's argument that Muramatsu is silent about gate and data pads, it is respectfully pointed out to applicant that since Muramatsu discloses that the lead lines are completely covered with package mold materials, one of ordinary skill in the art would easily understand that the pads are also covered with the mold material. Further, in Fig. 2, Muramatsu shows that the connection between the driver IC (15) and the lead lines (14) is also covered by the mold materials. Accordingly, it is clear that in Muramatsu the mold materials cover the pads as well the integrated circuits.

Therefore, the rejection was proper and thus maintained.

In response to applicant's comment that the objection of claims 6, 7, 21, 22 and 24 should be withdrawn since claims 1 and 17 are allowable, it is respectfully pointed

out to applicant that since claims 1 and 17 are still not found allowable based on the arguments, the objections (allowability) of claims 6, 7, 21, 22 and 24 are not withdrawn.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tarifur R. Chowdhury whose telephone number is (571) 272-2287. The examiner can normally be reached on M-Th 7:30-5:00; 1st Friday Off; 2nd Friday 7:30-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2871

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TRC
August 31, 2006



TARIFUR CHOWDHURY
Primary Examiner